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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Fratti et al.  
Case: 12-19  
Serial No.: 10/628,941  
Filing Date: July 29, 2003  
Group: 2811  
Examiner: Ori Nadav

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: Wen-Manning Date: November 29, 2005

Title: Techniques for Curvature Control in Power Transistor Devices

TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF

Mail Stop AF  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

- (1) Request to Reinstate Appeal; and
- (2) Supplemental Appeal Brief.

Please charge **Deposit Account No. 50-0762** to cover any fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully,

Kevin M. Mason

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(203) 255-6560

Date: November 29, 2005



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Signature: *Kevin M. Mason* Date: November 29, 2005

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REQUEST TO REINSTATE APPEAL

Mail Stop Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Arlington, VA 22313-1450

Sir:

Applicants hereby request to reinstate the appeal. Applicants' Appeal Brief was submitted on June 27, 2005. A new Office Action was mailed on September 2, 2005.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

*Kevin M. Mason*

Kevin M. Mason  
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Signature: *Gene Maurice* Date: November 29, 2005

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SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Appellants hereby reply to the non-final Office Action, mailed September 2, 2005. A request to reinstate the appeal is submitted herewith. Appellants' Appeal Brief in an Appeal of the final rejection of claims 1 through 16 in the above-identified patent application was submitted on June 27, 2005.

REAL PARTY IN INTEREST

The present application is currently assigned to Agere Systems Inc. Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

### STATUS OF CLAIMS

A statement identifying the original status of the claims is contained in Appellants' Appeal Brief. Claims 1-16 are pending in the above-identified patent application. Claims 1, 13 and 16 are the independent claims.

Each of claims 1-16 stands finally rejected under 35 U.S.C. §103(a). Claims 1-16 are appealed.

### STATUS OF AMENDMENTS

There have been no amendments to the claims filed subsequent to the appealed rejections.

### SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the claimed subject matter is contained in Appellants' Appeal Brief.

### STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the original grounds of rejection presented for review is contained in Appellants' Appeal Brief. In the present Office Action, Claims 1-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,091,121 issued to Oda, in view of S. Savastiouk et al., "Atmospheric Downstream Plasma," (hereinafter "Savastiouk") and U.S. Patent 6,559,011 issued to Shibib.

### CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

### ARGUMENT

In order to establish a *prima facie* case of obviousness, the following three criteria must be met:

[f]irst, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

M.P.E.P. §2143. Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references, and further, even if combinable, the references collectively do not teach each and every limitation of the independent claims.

#### Independent Claims 1, 13 and 16

The combined teachings of Oda with those of Savastiouk and Shibib do not teach or suggest a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device, a limitation present in each of independent claims 1, 13 and 16.

This has been Applicants' primary argument with respect to the prior combination of Hebert, Zommer and Savastiouk, as well. Nonetheless, the Examiner has not pointed to any portion of any cited reference that discloses this feature. In fact, other than copying the limitations of claim 1 in the rejection on page 3, the Examiner has not addressed this limitation at all in the current rejection.

The Examiner, beginning on the top of page 3 of the current Office Action, stated that,

Oda teaches in figures 102 and related text a method for controlling the curvature of a power transistor device comprising a device film formed on a substrate, the method comprising the steps of:

applying a stress compensation layer (e.g. layers 12, 15, 17) to a surface of the device film (any layer below them), the stress compensation layer having a tensile stress sufficient to

counterbalance at least a portion of the overall residual stress of the device.

Again, the Examiner has not provided any support for the allegation that Oda teaches “a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device.”

The Examiner has acknowledged that Oda does not teach the step of thinning the substrate, wherein a power transistor device having an overall residual stress attributable at least in part to the thinning step. The Examiner pointed to Savastiouk for teaching thinning the substrate. The Examiner further asserts that the combination is motivated by the teachings of Savastiouk who point out the advantages of using a thinner substrate.

While Savastiouk may teach an advantage that thinner substrates allow device manufacturers to “increase the number of die per wafer,” Savastiouk does not disclose or suggest that thinner wafers may be used to control curvature of a power transistor device, as taught by the present invention.

Thus, Applicants respectfully disagree with the Examiner’s assertions for at least the reason that there exists no motivation to combine the teachings of Oda with those of Savastiouk and Shibib, to come up with the limitations of the present invention. For example, with regard to the proposed combination of Oda and Savastiouk, the Examiner found it obvious to use the procedures of Savastiouk in Oda “to thin the substrate in Oda’s device.” See, Office Action, page 3. Applicants disagree and respectfully submit that one of ordinary skill in the art would not be motivated to supplement the teachings of Oda with those of Savastiouk to thin the substrate in Oda’s device, as the Examiner suggests, in order to control curvature of a power transistor device.

To the extent that Savastiouk suggests to thin a substrate, it is for an entirely different purpose. In addition, there is no suggestion in Savastiouk that the overall residual stress is attributable at least in part to the thinning step. While Savastiouk may include keywords of “residual stress” and “thinning,” Savastiouk does not suggest that the overall residual stress of a device is *attributable* to the thinning step. Therefore, it is the Applicants’ position that one of ordinary skill in the art would not be motivated to combine the teachings of Oda with those of Savastiouk.

Applicants respectfully further submit that the teachings of Oda, Savastiouk, and Shibib, even if combinable, in no way teach or suggest a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device attributable, at least in part, to a thinning of a substrate of the device. The Examiner's failure to provide any support for the allegation that Oda teaches "a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device," strongly suggests that it doesn't exist (especially when Applicants have consistently identified this limitation as a distinguishing feature in prior responses). Applicants can find no such teaching in Oda or elsewhere in the cited references.

Specifically, nothing in the combined teachings of the references in any way indicates that the layers 12, 15, 17 of Oda would have a tensile stress *sufficient to counterbalance* any amount of overall residual stress resulting from substrate thinning. Layers 12, 15, 17 of Oda are protecting nitride films. While Oda teaches a protecting insulator film having a compressive stress for relaxing a tensile stress of the protecting nitride film (see, e.g., Abstract), there is no suggestion that the tensile stress is *sufficient to counterbalance* any amount of overall residual stress resulting from substrate thinning. *In fact, it appears from the limited teachings of Oda that the protecting insulator film is merely present to compensate for stresses inherent in layers adjacent thereto.*

#### Claims 7 and 11-12

With regard to claim 7, this claim specifies that the steps (e.g., of claim 1) of thinning the substrate and applying a stress compensation layer are performed repeatedly until a desired curvature is attained. Applicants respectfully submit that the teachings of the cited references, even if combinable, do not teach or suggest this limitation.

In the present Office Action, page 4, the Examiner stated that it would have been obvious to monitor the curvature of the device by using an off-axis optical laser technique and to repeat the steps of thinning and applying until a desired curvature is attained." Applicants respectfully submit that these statements by the Examiner are incorrect. The cited references do not disclose that thinning of the substrate would produce a curvature of the device as the Examiner contends.



Claims 9 and 10

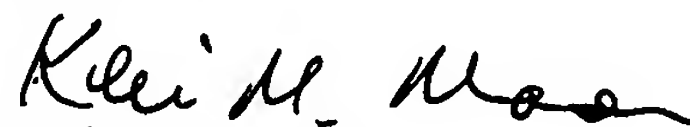
Claim 9 specifies that the stress compensation layer applied to the surface of the device changes the curvature of the device. Claim 10 specifies that the stress compensation layer applied to the surface of the device maintains the curvature of the device. The Examiner asserts that this is inherent in the prior art device. While Oda may teach a protecting insulator film having a compressive stress for relaxing a tensile stress of the protecting nitride film, there is no suggestion that a stress compensation layer applied to the surface of the device changes or maintains the *curvature* of the device.

Conclusion

In conclusion, it is believed that the §103(a) rejections of claims 1-16 are improper and should be withdrawn.

In view of the foregoing, Applicants believe that claims 1-16 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejections.

Respectfully submitted,



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Dated: November 29, 2005



CLAIMS APPENDIX

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.